

**UNIVERSITY INSTITUTE OF ENGINEERING & TECHNOLOGY
PANJAB UNIVERSITY, CHANDIGARH - 160014**

FACULTY PROFILE

1. Name : Garima Joshi
2. Designation : Assistant Professor
3. Department : Electronics & Communication Engineering
4. Contact No. : 9815943229
5. Email id : joshi_garima5@yahoo.com
6. Research Areas : Image Processing and VLSI Design
7. Educational Background :



S. No	Degree	University/ Institution	Year of Pass	% of Marks	Class
1.	M.E (Electronics and Communication)	Punjab University (UIET), Chandigarh	2008	74.2%	I Class
2.	B.Tech (Electronics and Communication)	Himachal Pradesh University, Shimla	2002	76.7 %	With Honors
3.	Diploma in Electronics and Communication Engineering (3 Years)	Himachal Pradesh Takniki Shiksha Board	1999	76%	I Class
4.	Matriculation	D.A.V Public School, Solan (Affiliated to CBSE)	1996	75.6%	I Class

8. Experience:

S. No.	Period		Organization / Institution	Position Held
	From	To		
1.	<i>Aug 2009</i>	<i>Till date</i>	UIET, Panjab University	Assistant Professor (ECE)
2.	<i>Nov 2007</i>	<i>June 2009</i>	UIET, Panjab Universit	Project Associate
3.	<i>Oct 2004</i>	<i>Aug 2006</i>	National Hydroelectric Power Corporation (NHPC), Parbati 800 MW Hydro Electric Project - II, Distt. Kullu (Himachal Pradesh)	Engineer (E&C)
4.	<i>August 2003</i>	<i>Oct 2004</i>	Institute of Engineering and Emerging Technologies (IEET), Baddi, Himachal Pradesh Department of Electronics and Communication Engineering	Lecturer

9. List of Publications:

International Journals:

1. Garima Joshi and Amit Choudhary, "Analysis of Short Channel Effects in Nanoscale MOSFETs", International Journal of Nanoscience, vol.10, no.1, pp. 275-279, 2010.
2. Amit Chaudhry, J.N. Roy and Garima Joshi, "Nanoscale Strained-Si MOSFET Physics and Modeling Approaches: A Review", International Chinese Journal of Semiconductors, vol.31, no.10, pp. 400-1 to 400-6, 2010.
3. Garima Joshi, Manjinderpal Singh, and Monica Chauhan, "Analysis of gate tunneling currents in nanoscale metal-oxide-semiconductor field effect transistors (MOSFETs) with SiO₂ and high-K gate dielectrics" Proc. IMechE Vol. 223 Part N: J. Nanoengineering and Nanosystems, vol.223, no.1, pp. 19-24, 2010.(IF=0.6)
4. Amit Chaudhry, Garima Joshi, J. N. Roy, and D.N. Singh, "Strained Silicon MOSFET Structures for Nanoscale Applications: A Review", Acta Technica Napocensis", vol.51, no.1, pp. 15-21, 2010.

5. S. B. Rahi and Garima Joshi, "Analytical Model of Surface Potential and Threshold Voltage of Biaxial Atrained Silicon NMOSFET Including QME", vol. 5, no. 1, pp.601-607, 2012
6. S. B. Rahi, Garima Joshi, "A Physics Based Model Of Inversion Charge Sheet (Ics) For Nanoscale Biaxial Strained-Silicon NMOSFET Including Quantum Mechanical Effect (QME), International Journal of Advances in Engineering & Technology, vol. 5, no. 2, 2012

Conferences

7. G Khurana, Garima Joshi, J Kaur, "Static hand gestures recognition system using shape based features" Engineering and Computational Sciences (RAECS), Recent Advances in, 1-4, 2014.
8. Jatinderpal Kaur, Garima Joshi, Rajneet Kaur, "Vision based Hand Gesture Recognition System for ISL", 3rd International Conference on Biomedical Engineering & Assistive Technologies, Chandigarh, 2014.
9. Garima Joshi, "Nanoscale MOSFETs: An Overview of Short Channel Effects and Novel Channel Material" ICSCI 2008, International Conference on Systemics, Cybernetics and Informatics, Hyderabad, pp. 1-5, August 2008.
10. Garima Joshi, D.N. Singh, and Sharmelee Thangjam, "Effect of temperature variation on Gate Tunneling currents in nanoscale MOSFETs" Published in the proceedings 8th International Conference on nanotechnology IEEE NANO, Arlington Texas, US, pp. 37-41, August 2008.
11. Garima Joshi, Manjinderpal Singh, and Monica Chauhan, "Analysis of Gate Tunneling Current Density in Nanoscale MOS Structures" International Conference on Wireless Networks and Embedded Systems, 2008.
12. Garima Joshi, "Mobile Evolution Towards 3G" COIT-2007, RIMT Mandigobindgarh, 2007.

10. Projects/Consultancy Work:

Completed a DIT sponsored Project titled "Modeling and Simulation of nanoscale MOSFETs at Room temperature and Classical MOSFET at Liquid Nitrogen Temperature (LNT)" of Rs. 24.5 Lacs of duration of 3years